AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (Currently Amended) A signal processing semiconductor integrated circuit comprising:

a reception circuit including a first low noise amplifier that amplifies a ~~reception~~ received signal, a frequency ~~conversion means~~ converter that synthesizes an amplified signal and an oscillation signal ~~of a specific frequency~~ to form a frequency converted signal from the amplified received signal, and a ~~second~~ signal amplifier, coupled to ~~direct current coupled with~~ the frequency ~~conversion means~~ converter, ~~which~~ that amplifies the frequency converted signal ~~by the frequency conversion means~~; and

a ~~third~~ second low noise amplifier, having an input terminal electrically isolated from the received signal, that is activated while the first low noise amplifier is deactivated~~, whose input terminal is not connected to an external terminal to which the reception signal is inputted~~ to calibrate an offset of the signal amplifier.

2. (Currently Amended) A signal processing semiconductor integrated circuit according to Claim 1, wherein the input terminal of the ~~third~~ second low noise amplifier ~~has~~ is coupled to an impedance ~~connected which~~ that is equivalent

to that of an external circuit ~~connected to the~~ coupled to an input terminal of the first low noise amplifier.

3. (Currently Amended) A signal processing semiconductor integrated circuit comprising:

a reception circuit including a first amplifier that amplifies a ~~reception~~ received signal, a frequency ~~conversion means~~ converter that synthesizes an amplified signal and an oscillation signal ~~of a specific frequency~~ to form a frequency converted signal from the amplified received signal, and a second amplifier, coupled to ~~direct current coupled with~~ the frequency ~~conversion means~~ converter, ~~which~~ that amplifies the frequency converted signal ~~by the frequency conversion means~~, and having a first operation mode in which the reception circuit is activated, and a second operation mode in which the reception circuit is deactivated; and

a third amplifier ~~of which~~ having an input terminal that is not connected to an external terminal to which the reception signal is inputted,

wherein the second amplifier is provided with a calibration circuit that calibrates a direct current offset of the second amplifier, and

wherein the first amplifier is deactivated, ~~and~~ the third amplifier is activated ~~in response to shifting from the second operation mode into the first operation mode,~~ and the calibration circuit calibrates the direct current offset of the second amplifier in response to shifting from the second operation mode to the first operation mode.

4. (Currently Amended) A signal processing semiconductor integrated circuit according to Claim 3, wherein the input terminal of the third amplifier ~~has~~ is connected to an impedance ~~connected which~~ that is equivalent to that of an external circuit connected to ~~the~~ an input terminal of the first amplifier.

5. (original) A signal processing semiconductor integrated circuit according to Claim 3, wherein the third amplifier is deactivated and the first amplifier is activated, after the direct current offset is calibrated.

6. (Currently Amended) A signal processing semiconductor integrated circuit according to Claim 5, wherein the second amplifier has ~~plural~~ a plurality of amplifier stages[[,]] and ~~the amplifier stages each are provided with the~~ a plurality of calibration circuits are provided that calibrate the direct current offsets of the amplifier stages.

7. (Currently Amended) A signal processing semiconductor integrated circuit ~~formed on one semiconductor substrate, comprising: the reception circuit~~ according to Claim 3[[;]], further comprising:

a transmission circuit that includes a modulation circuit that modulates a transmission signal, and an up-converting frequency ~~conversion means~~ converter that synthesizes a modulated signal and an oscillation signal to convert them into a higher frequency signal;

a control circuit that controls the reception circuit and the transmission circuit; and

an oscillation circuit that generates the oscillation signals synthesized by the reception circuit and the transmission circuit~~, or an oscillation control signal~~.

8. (Currently Amended) A wireless communication system comprising:

the signal processing semiconductor integrated circuit according to Claim 7; and

a base band circuit, formed on a semiconductor substrate, ~~which implements a signal processing, namely a conversion from a reception~~ to convert a base band signal into an audio signal, to convert ~~and a conversion from~~ the audio signal into the base band signal, and ~~a~~ to control ~~of~~ the signal processing semiconductor integrated circuit,

wherein the base band circuit supplies ~~the signal processing semiconductor integrated circuit with~~ a first command ~~signal~~ to activate a reference voltage generation circuit that generates a bias voltage to a current source for supplying operation currents to the frequency ~~conversion means~~ converter and the second amplifier, and a second command ~~signal~~ to activate the frequency ~~conversion means~~ converter and the second amplifier.

9. (Currently Amended) A wireless communication system according to Claim 8, wherein the first command ~~signal~~ to activate the reference voltage generation circuit and the second command ~~signal~~ to activate the frequency ~~conversion means~~ converter and the second amplifier are supplied from the

base band circuit to the control circuit ~~inside the signal processing semiconductor integrated circuit~~.

10. (Currently Amended) A ~~control method in a~~ signal processing semiconductor integrated circuit[[:]] comprising:

a reception circuit including a ~~fist~~ first amplifier that amplifies a ~~reception~~ received signal, a frequency ~~conversion means~~ converter that synthesizes an amplified signal and an oscillation signal ~~of a specific frequency~~ to form a frequency converted signal from the amplified received signal, and a second amplifier, direct current-coupled ~~with~~ to the frequency converter, that ~~conversion means which,~~ amplifies the frequency converted signal ~~by the frequency conversion means~~, and a third amplifier ~~of which~~ having an input terminal that is not connected to an external terminal to which the ~~reception~~ received signal is inputted; and having a first operation mode in which the reception circuit is activated, and a second operation mode in which the reception circuit is deactivated,

wherein ~~the~~ a direct current offset of the second amplifier is calibrated in a state ~~that~~ in which the first amplifier is deactivated and the third amplifier is activated in response to shifting from the second operation mode into the first operation mode.

11. (New) A signal processing semiconductor integrated circuit according to Claim 2, further comprising offset canceling circuitry coupled to the signal amplifier to cancel the offset of the signal amplifier.

12. (New) A signal processing semiconductor integrated circuit according to Claim 11, wherein an output terminal of the second low noise amplifier is coupled to the frequency converter.

13. (New) A signal processing semiconductor integrated circuit according to Claim 11, wherein the signal amplifier includes a plurality of amplifier circuits, and the offset canceling circuitry includes a plurality of offset canceling circuits each of which is coupled between an input terminal and an output terminal of one of the plurality of amplifier circuits.

14. (New) A signal processing semiconductor integrated circuit according to Claim 1, wherein the first low noise amplifier, the second low noise amplifier, the signal amplifier and the frequency converter are formed a single chip.

15. (New) A signal processing semiconductor integrated circuit according to Claim 6, wherein the first amplifier includes a low noise amplifier.

16. (New) A signal processing semiconductor integrated circuit according to Claim 15, wherein an output terminal of the third amplifier is coupled to the frequency converter.

17. (New) A signal processing semiconductor integrated circuit comprising:

a reception circuit including a low noise amplifier that amplifies a received signal, a frequency converter that

synthesizes an amplified signal and an oscillation signal to form a frequency converted signal from the amplified received signal, a first amplifier coupled to the frequency converter to amplify the frequency converted signal, and an offset calibrating circuit coupled to the first amplifier to calibrate an offset of the first amplifier; and

a second amplifier having an input terminal that is electrically isolated from the received signal,

wherein the reception circuit has a first operation mode in which the reception circuit is activated, and a second operation mode in which the reception circuit is deactivated,

wherein the low noise amplifier is activated and the second amplifier is deactivated in the first operation mode, and

wherein the low noise amplifier is deactivated, the second amplifier is activated and the offset of the first amplifier is calibrated by the offset calibrating circuit, in response to shifting from the second operation mode to the first operation mode.

18. (New) A signal processing semiconductor integrated circuit according to Claim 17, wherein an output terminal of the second amplifier is coupled to the frequency converter.

19. (New) A signal processing semiconductor integrated circuit according to Claim 17, further comprising an impedance coupled to the input terminal of the second amplifier.

20. (New) A signal processing semiconductor integrated circuit according to Claim 17, wherein the second amplifier is coupled to the frequency converter.

21. (New) A signal processing semiconductor integrated circuit according to Claim 7, and formed on one semiconductor substrate.